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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,990	03/07/2005	**Shridhar Mubaraq Mishra**	1890-0213	6999

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EXAMINER	
RUTKOWSKI, JEFFREY M	

ART UNIT	PAPER NUMBER
2473	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,990	MISHRA ET AL.	
	Examiner	Art Unit	
	JEFFREY M. RUTKOWSKI	2473	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-17,19-25 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-17,19-25 and 28-30* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7, 18 and 26-27 have been cancelled.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/30/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 8-11, 16-17, 19, 24, 25, 28, 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzeng et al. (US Pg Pub 2003/0212815), hereinafter referred to as Tzeng, in

view of Moran et al. (US Pg Pub 2002/0071398), hereinafter referred to as Moran, Takeuchi et al. (US Pat 5,233,603), hereinafter referred to as Takeuchi.

5. For **claims 8, 17, 24, 28 and 29**, Tzeng discloses a plurality of Media Access Control (MAC) interfaces (MACs **101 and 106**; see figure 1), each MAC interface is configured to receive/transmit Fast Ethernet (FE) packets (figure 1 shows the MACs **101 and 102** have bi-directional interfaces that transmit and receive Fast Ethernet packets), at least one of the MAC interfaces (MAC **101**) further being configured to receive/transmit Gigabit Ethernet (GE) packets independent of the other plurality of MAC interfaces (MAC **106**; figure 1 shows the MAC **101** transmits and receives GE packets independently of the other MAC **106**) and wherein the ingress/egress port (chip 0; see figure 3) operates as a single GE physical port in a first mode of operation (when the MACs **101 and 106** are operating at FE speeds the SERDES GMAC is the only port operating as a physical GE port; see figure 1) and as more than one FE physical port in a second mode of operation (in an 8+2 configuration, the MAC **106** is used to provide connectivity for 8 FE ports; see paragraph 0021 and figure 1).

6. Tzeng discloses the use of a single packet buffer **103** that is used to transmit and receive packets from all the interfaces (see figure 1). Tzeng does not disclose the use of transmit and receive modules. Moran discloses receive (receive store **30** allocated in memory **14**; see paragraph 0032) and transmit modules (transmit store **29** allocated in memory **14**; see paragraph 0032) which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces (figure 1 shows a bus is used to send and receive information between memory **14** and all the MAC interfaces **14**) and wherein each MAC interface is associated with a separate buffer configured to store packets as they are received at

the respective MAC interface (see paragraph 0032). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Moran's arrangement in Tzeng's invention to control the amount of bandwidth for a port (Moran, title).

7. The combination of Tzeng and Moran discloses the use of a receive module. The combination of Tzeng and Moran does not disclose how packets are read from memory **14** (see figure 1 of Moran). Takeuchi discloses the receive module (buffer units **2501**-250N; see figure 4) being arranged to receive packets from the respective buffers sequentially (the buffer units **2501-250N** sequentially receive packets from input buffers **1401** to **140N** sequentially; see col. 6 lines 9-11). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Takeuchi's arrangement in Tzeng's invention to multiplex the received information (Takeuchi, col. 6 lines 9-11).

8. Specifically for **claim 17**, Tzeng discloses the use of at least one ingress/egress port (chip 0; see figure 3).

9. Specifically for **claims 24 and 28**, Tzeng suggests a switch configured to switch the ingress/egress port (chip 0) between a first mode (mode where MACs **101 and 106** are both operating on FE packets) and a second mode of operation (8+2 configuration; see paragraph 0021) for the ingress/egress port (chip 0; this feature is suggested because figure 1 shows the MAC **101** can operate at either FE or GE speeds depending the type of PHY **108** that is attached).

10. For **claim 9**, Tzeng discloses wherein only one of the MAC interfaces is configured to receive/transmit both GE and FE packets (figure 1 shows the MAC **101** has an interface that can receive and transmit both GE and FE packets), the other MAC interfaces (interface for MAC

106) only being adapted to receive/transmit FE packets (figure 1 shows the MAC **106** has an interface for sending and receiving only FE packets).

11. For **claims 10 and 11**, the combination of Tzeng and Moran discloses the use of a receive module. The combination of Tzeng and Moran does not disclose the sequential reception of FE packets. Takeuchi suggests wherein the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously (the packets are read from the input buffers **1401** to **140N** in a cyclical manner; see col. 6 lines 5-11). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Takeuchi's arrangement in Tzeng's invention to multiplex the received information (Takeuchi, col. 6 lines 9-11).

12. For **claim 16**, Tzeng discloses wherein the plurality of MAC interfaces consists of 8 MAC interfaces (this feature is suggested by Tzeng because an 8+2 switch arrangement has 8 FE ports; see paragraph 0021, figure 1 and figure 3).

13. For **claim 19**, Tzeng discloses wherein the at least one ingress/egress port (figure 3 shows there are three chips 0 through 2 chained together) comprises eight ingress/egress ports (each chip provides at least 8 ports; see paragraphs 0023-0024 and figure 3), each ingress/egress port (chip 0 through 2) being configured to switch between a first mode (when the MAC **101** and the MAC **106** are operating at FE speeds; see figure 1) and a second mode (8+2 switch arrangement; see paragraph 0021), in which each ingress/egress port (chip) operates as a single GE physical port in the first mode (when the MACs **101 and 106** are operating at FE speeds, the SERDES MAC is the only port operating as a physical Gigabit port; see figure 1) and as eight FE physical ports in the second mode (in the 8+2 arrangement the MAC **106** provides

connectivity for 8 FE ports; see paragraph 0021) and wherein the switch can operate as n GE ports and 8(8-n) FE ports for n a selectable integer in the range 0 and 8 (Tzeng's invention also has this capability because Tzeng's invention can support any number of interfaces; see paragraph 0023).

14. For **claim 25**, Tzeng suggests providing a control signal (auto-negotiation signal) to determine whether the MAC interfaces operate as FE interfaces or whether the at least one MAC interface operates as a GE interface (figure 1 shows the MAC interface **101** auto-negotiate FE or GE interface speeds).

15. **Claims 12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzeng in view of Moran and Takeuchi as applied to **claims 8 and 17 respectively** above, and further in view of Gentry, Jr. (US Pat 6,356,951), hereinafter referred to as Gentry.

16. For **claims 12 and 20**, the combination of Tzeng, Moran and Takeuchi, discloses the receive module further includes a memory configured to store packet data (Moran, paragraph 0032).

17. The combination of Tzeng, Moran and Takeuchi does not teach the use of a receiver that interfaces with a parser. Gentry discloses an input port processing module 104 interfaces with a header parser 106 [figure 1A]. The header parser 106 parses only the header (descriptor) portion of the packets [col. 7 lines 50-55] (a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a receiver interface in Tzeng's invention to identify related packets (Gentry, col. 7 line 53).

18. **Claims 13-15, 21-23 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzeng in view of Moran, Takeuchi and Gentry as applied to **claim 12 and 20** above, and further in view of Di Placido (US Pat 6,226,292).

19. For **claims 13, 15, 21, 23**, the combination of Tzeng, Moran, Takeuchi and Gentry teach a receiver interface for fetching data the header parser **106** copies header information (descriptor) from input port processing module **104** into a header memory **302 [Gentry, col. 17 lines 8-9 and figure 3]** (claim 13: wherein the receiver interface is further configured to fetch packet data from the set of buffers and store the packet data in the memory; claim 15: wherein the receiver interface is further configured to store the descriptor associated with the packet data in the memory).

20. The combination of Tzeng, Moran, Takeuchi and Gentry do not disclose the use of more than one receive buffers (set of buffers). Di Placido teaches a switch arrangement that contains more than one set of receive buffers **20 [figure 2]**. It would have been obvious to a person of ordinary skill in the art to use a set of buffers in Tzeng's invention to manage memory space by a particular buffer to a particular MAC interface **[Di Placido, col. 4 lines 62-65]**.

21. For **claims 14 and 22**, Tzeng does not disclose the use of FIFO buffers. Takeuchi teaches the use of First-In-First-Out (FIFO) buffers to receive information **[see col. 8 lines 5-15]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Takeuchi's arrangement in Tzeng's invention to use a buffer structure that is available in the marketplace (Takeuchi, col. 8 lines 5-15).

22. For **claim 30**, the combination of Tzeng, Moran and Takeuchi do not teach the use of a receiver that interfaces with a parser. Gentry discloses a parser (header parser **106**) for

extracting information form headers in the received packets (the header parser **106** parses the header portions of the packets; see col. 7 lines 50-65), and adding this information to the descriptor (this feature is suggested by Gentry because the header parser **106** can also extract other information from the packet, such as the packet length; see col. 8 lines 14-20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Gentry's arrangement in Tzeng's invention to identify related packets **[Gentry, col. 7 line 53]**.

Response to Arguments

23. Applicant's arguments with respect to **claims 8-17, 19-25 and 28-30** have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

24. **Claim 31** is still objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The reasons for allowance were cited in the final action mailed on 09/30/2010.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Tzeng reference has been reintroduced because the claims do not required the claimed modes of operation to be mutually exclusive (i.e. either a plurality of FE ports is provided or a single GE port is provided). However, Chang et al. (US Pat 6,731,631) teaches such a feature where an ingress/egress port (port controller) operates as either a plurality of FE ports in a first mode of operation (version) or as a single GE port in a second mode of operation (second version; see col. 7 lines 50-60 and figures 3-4).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey M Rutkowski/
Examiner, Art Unit 2473

/KWANG B. YAO/

Supervisory Patent Examiner, Art Unit 2473